

CLAIMS

What is claimed is:

1. A method of inhibiting metal silicide encroachment in a transistor, the method comprising:
  - 5 depositing a metal layer over a transistor structure;
  - performing a silicidation anneal to form metal silicide regions of terminals of the transistor structure at a first temperature sufficiently low to inhibit lateral encroachment of the metal silicide regions;
  - 10 selectively removing unsilicided portions of the metal layer from over the transistor; and
  - implanting encroachment inhibiting ions into the transistor after selectively removing the unsilicided portions of the metal layer.
- 15 2. The method of claim 1 further comprising:
  - performing another silicidation anneal after implanting the encroachment inhibiting ions.
3. The method of claim 2 wherein the step of performing another silicidation anneal 20 after implanting the encroachment inhibiting ions is performed at a second temperature not substantially lower than the first temperature.
4. The method of claim 2 wherein the first temperature is not substantially greater than 400°C; and 25 the performing of the silicidation anneal after implanting the encroachment inhibiting ions is performed at a second temperature not substantially less than 400°C.
5. The method of claim 1 wherein the first temperature is not substantially greater than 400°C.
- 30 6. The method of claim 1 wherein metal comprising the metal layer comprises at least one of cobalt or nickel, and the metal silicide regions comprise a corresponding at least one of cobalt silicide or nickel silicide.

7. The method of claim 1 further comprising:
  - selecting an encroachment inhibiting ion type;
  - determining an ion dose before implanting the encroachment inhibiting ions;
  - 5 and
  - determining an ion energy before implanting the encroachment inhibiting ions.
8. The method of claim 7 wherein the encroachment inhibiting ions are selected from the group consisting of nitrogen-based ions, fluorine-based ions and hydrogen-based ions.
- 10
9. The method of claim 7 wherein the encroachment inhibiting ions comprise dinitrogen.
10. The method of claim 9 wherein the ion dose is determined to be less than  $2 \times 10^{15}$  ions/cm<sup>2</sup>.
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11. The method of claim 10 wherein the ion dose is determined to be greater than  $1 \times 10^{14}$  ions/cm<sup>2</sup>.
12. The method of claim 10 wherein the ion dose is determined to be greater than  $1 \times 10^{15}$  ions/cm<sup>2</sup>.
- 20
13. The method of claim 9 wherein the ion energy is determined to be less than 10keV.
14. The method of claim 13 wherein the ion energy is determined to be greater than 1keV.
- 25
15. The method of claim 13 wherein the ion energy is determined to be greater than 3keV.
16. The method of claim 1 wherein the step of performing the silicidation anneal comprises performing a rapid thermal anneal.

17. A method of improving thermal stability of a metal silicide to decrease encroachment on a transistor channel in a transistor, the method comprising:

depositing a metal layer over the transistor;

5 performing a silicidation anneal within a first temperature range to form metal silicide regions of transistor terminals of the transistor;

selectively removing unsilicided portions of the metal layer from over the transistor;

implanting encroachment inhibiting ions into the transistor terminals after

10 selectively removing the unsilicided portions of the metal layer; and

performing a silicidation anneal within a second temperature range after

implanting the encroachment inhibiting ions, the first temperature range including temperatures below temperatures in the second temperature range.

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18. The method of claim 17 further comprising:

selecting the first temperature range to be sufficiently low to protect against lateral metal silicide mobility; and

20 selecting the second temperature range to be sufficiently high to substantially complete metal silicidation.

19. The method of claim 17 wherein the transistor terminals comprise a gate terminal and source/drain terminals.

25 20. The method of claim 17 wherein metal within the metal layer comprises nickel and the metal silicide regions comprise nickel silicide.

21. The method of claim 17 wherein the encroachment inhibiting ions comprise dinitrogen gas ions.

22. The method of claim 21 further comprising:

selecting a dinitrogen ion dose having a value between  $1 \times 10^{14}$  and  
 $2 \times 10^{15}$  molecules/cm<sup>2</sup>; and

5 selecting a dinitrogen energy between 1keV and 10keV.

23. The method of claim 22 wherein the dinitrogen ion dose is selected to be about  
 $5 \times 10^{14}$  ions/cm<sup>2</sup>.

10 24. The method of claim 22 wherein the dinitrogen energy is selected to be about 5keV.

25. The method of claim 17 further comprising:

forming a protection layer over the metal layer after depositing the metal layer  
and before selectively removing the unsilicided portions of the metal  
15 layer.

26. The method of claim 25 wherein the metal layer comprises nickel and the protection  
layer comprises titanium nitride.

27. A method of improving thermal stability of nickel silicide and inhibiting formation of nickel disilicide in a channel region of a transistor, the method comprising:

5 forming a transistor structure including three transistor terminals;

forming nickel over each of the three transistor terminals;

heating the transistor structure at a temperature in a first temperature range

sufficiently high to form nickel silicide regions of the three transistor

terminals and sufficiently low to inhibit lateral encroachment of the

nickel silicide regions;

10 implanting encroachment inhibiting ions into the nickel silicide regions of the

three transistor terminals after heating the transistor structure in the

first temperature range; and

heating the transistor structure at a temperature in a second temperature range

after implanting the encroachment inhibiting ions, the first temperature

15 range including temperatures below temperatures in the second

temperature range.

28. The method of claim 27 wherein the step of forming nickel over each of the three  
transistor terminals comprises:

20 sputtering a layer of nickel over the transistor structure before heating the  
transistor structure; and

wet etching unsilicided portions of the layer of nickel from over non-terminal  
portions of the transistor structure after heating the transistor structure.